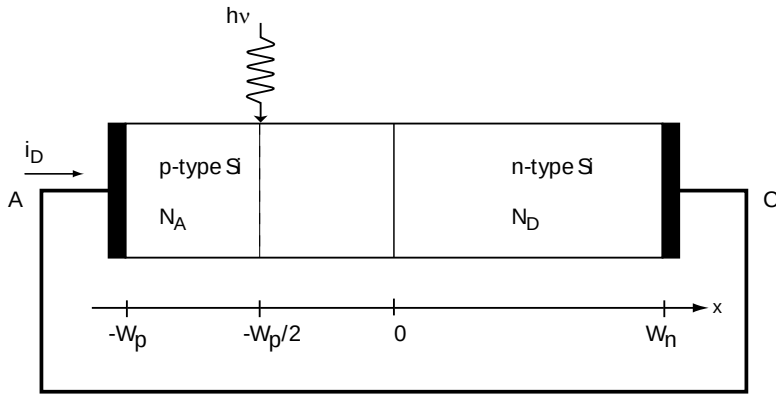
Problem Set #8

Assigned: Wednesday, October 29, 2008
Due: Wednesday, November 5, 2008 at recitation

Reading Assignments:	10/23/08	Sections 6.3 - 6.4 of Howe & Sodin
	10/28/08	Sections 7.1 - 7.2 of Howe & Sodini
	10/30/08	Sections 7.3 – 7.5 of Howe & Sodini
	11/04/06	Sections 8.1 – 8.5 of Howe & Sodini

PLEASE WRITE YOUR RECITATION SESSION TIME ON YOUR PROBLEM SET SOLUTION

1. [20 points] Diode with Light generation (Structure used in solar cells and imagers).



$N_A = 10^{19}$ cm^{-3}
$N_D = 10^{17}$ cm^{-3}
$D_n = 10$ cm^2/s
$D_p = 5$ cm^2/s

The p-n diode shown above is illuminated by light which generates G_L hole electron pairs per second in the plane at $x = -W_p/2$. This illumination results in an increased electron & hole population at $x = -W_p/2$. You are not given G_L, but you are told that $n'_p(-W_p/2) = [n_p(-W_p/2) - n_{po}] = 10^{11}$ electrons / cm^3.

The diode is short-circuited and there is no recombination except at the contacts. Assume that $[n_p(x) - n_{po}] << N_A$ and $[p_n(x) - p_{no}] << N_D$, and assume quasi-neutrality except in the space charge layer. Assume that the diffusion coefficients of electrons and holes are D_n and D_p as indicated in the figure above.

a. What are the minority carrier concentrations at the following positions? $x=-W_p$, $-x_p$, x_n & W_n?
b. Sketch the minority carrier concentrations everywhere in the diode?
c. Sketch the minority carrier current densities throughout this device, i.e., $J_n(x)$ for $-W_p < x < 0$, and $J_p(x)$ for $0 < x < W_n$
d. Calculate the total diode current density, J_D.
e. What is the value of G_L?

2. [30 points] An npn transistor with emitter area A_E = 2.5 μm X 2.5 μm is biased in the forward active region, with the collector current I_C = 50 μA. The emitter, base and collector dimensions and doping are: $N_{dE} = 10^{19}$ cm^{-3}, W_E = 0.3 μm, $N_{aB} = 10^{17}$ cm^{-3}, W_B = 0.25 μm, and $N_{dC} = 10^{16}$ cm^{-3}, W_C = 1.5 μm.

a. Find the base-emitter bias V_{BE}.
b. Sketch the minority carrier concentrations in the emitter and base.
c. Find the base current I_B.

Given the npn transistor with the parameters and operating point above, with the additional information that the Early Voltage, V_{An} = 25 V.

d. Find the transconductance g_m, the input resistance r_π, and the output resistance r_o.

Given the npn transistor with the parameters and operating point above, with the additional information that the emitter-base depletion width is x_{BE} = 0.05 μm.

e. What is the minority electron charge storage $Q_{NB}(V_{BE})$ at this operating point?
f. What is C_π at this operating point?
g. At what frequency does $|1/j\omega C_\pi| = r_\pi$?

3. [25 points] In some special purpose technologies, a vertical pnp transistor with the same structure and layout as the npn shown in lecture (Figure 7.1 of H&S) is available, except that the contact to the emitter is made using aluminum. The vertical pnp bipolar transistors has the following parameters:
Emitter: $N_{aE} = 1 \times 10^{19}$ cm^{-3}, W_E = 200 nm
Base: $N_{dB} = 8 \times 10^{16}$ cm^{-3}, W_B = 250 nm
Collector: $N_{aC} = 8 \times 10^{15}$ cm^{-3}, W_C=0.75 μm.
Emitter Area = A_E = 2.5 μm x 2.5 μm

a. Sketch the majority and minority carrier concentrations in equilibrium on a semi-log plot.
b. The device is now biased such that I_C = 100 μA and V_{CE} = -2 V. Sketch the minority carrier concentration for the bias condition. Neglect recombination in the emitter, base and collector quasi-neutral regions.
c. What is the total minority carrier charge stored in the base under the bias conditions in (b).
d. The device is now biased such that I_C = 50 μA and V_{CE} = -0.1 V. Sketch the minority carrier concentration for the bias condition. Neglect recombination in the emitter and base quasi-neutral regions.
e. What is the total minority carrier charge stored in the base under the bias conditions in (d).
f. Derive an appropriate large signal equivalent circuit model for the bias condition in (d) starting form the modified Ebers-Moll model presented in lecture

4. [25 points] **DC SPICE parameter extraction of an npn bipolar Junction Transitor**

This is an exercise in which you will use the ***Web-based Microelectronic Device Characterization*** system to characterize an npn BJT (http://iLab.mit.edu). From the measurements, you will also extract a model and a few DC SPICE parameters of the transistor in this problem set. The remaining DC SPICE parameters will be extracted in the next Problem Set. The User Manual is available on the ***iLab*** homepage.

In this problem, you will characterize an npn Bipolar Junction Transistor. Select one of the devices labeled "**2N3904**" under the "**Devices**" Menu. Take the measurements specified below and download the data to your local machine for additional graphing and further analysis. *Only download the data when you have satisfactory results*.

For the following measurements, hold V_{BE} between 0 and 0.75 V, and V_{CE} between 0 and 4 V. When relevant, vary I_B between 0 and 100 μA. For the SPICE parameter determination you will need the following structural information about the transistor. The gate length of this transistor is L = 3 μm, and the gate width is W = 20 μm. In this exercise, we do not distinguish between L and L_{eff} (see Section 4.6.1 in Howe & Sodini).

Below is the characterization assignment.

a. (5 points) Measure the ***output characteristics*** of the transistor. These are I_C vs. V_{CE} measurements with I_B as the stepping parameter. Download the data to your local machine and plot the ***output characteristics*** using your favorite software tool. Turn in a printout of this graph.

b. (5 points) Measure the ***transfer characteristics*** of the transistor. These are I_C & I_B vs. V_{BE} measurements with V_{CE} as the held constant and V_{CE} = 4.0 V. Download the data to your local machine and plot the ***transfer characteristics*** using your favorite software tool. Turn in a printout of this graph.

c. (5 points) Measure the ***Current Gain Characteristics in the forward active regime*** of the transistor. That is, b_F vs. I_C measurements for V_{CE} = 4 V. Download the data to your local machine and plot the ***Current Gain Characteristics characteristics*** using your favorite software tool. Turn in a printout of this graph.

d. (10 points) From the ***plots***, extract the SPICE parameters, **IS**, **BF** and **VAF** for the transistor (see Chapter 7 Howe & Sodini Table 7.1). The SPICE parameter determination should not demand extensive numerical analysis. There is no need to do regressions or least-squares fits.